WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a transistor formed in a well region of a semiconductor substrate, wherein the well region and the semiconductor substrate are of the same conductivity type; and

a buried layer formed within the substrate below the well region, wherein the buried layer is of opposite conductivity type than the well region, and wherein the buried layer includes a first portion underlying the transistor and a second portion spaced apart from and laterally surrounding the first portion.

2. The integrated circuit as recited in claim 1, further comprising a doped annular region of opposite conductivity type as the well region and extending past the well region to contact the second portion of the buried layer.

3. The integrated circuit as recited in claim 2, wherein the doped annular region laterally surrounds the transistor without surrounding other transistors of the integrated circuit.

4. The integrated circuit as recited in claim 1, wherein the first and second portions of the buried layer are separated by a distance of less than about 5 microns.

5. The integrated circuit as recited in claim 4, wherein the first and second portions of the buried layer are separated by a distance of approximately 1.2 microns.

6. The integrated circuit as recited in claim 2, further comprising one or more contact diffusions within the well region adapted for making contact to the well region.

7. The integrated circuit as recited in claim 6, wherein said one or more contact diffusions comprises a contact diffusion laterally adjacent to and in contact with the source region.

8. The integrated circuit as recited in claim 6, wherein said one or more contact diffusions comprises an annular contact diffusion arranged laterally within the doped annular region and laterally surrounding the transistor.

9. The integrated circuit as recited in claim 6, further comprising a contact to the doped annular region.

10. The integrated circuit as recited in claim 9, further comprising metallization adapted to connect the well region and the doped annular region to opposite polarities of a supply voltage.

11. The integrated circuit as recited in claim 2, further comprising an annular dielectric isolation region laterally surrounding the transistor.

12. The integrated circuit as recited in claim 1, wherein the transistor is an output transistor for the integrated circuit.

13. The integrated circuit as recited in claim 1, further comprising one or more analog circuit portions.

14. A method for forming an integrated circuit, said method comprising:

forming a doped structure within a semiconductor substrate, wherein the doped structure has opposite conductivity type than the substrate, and wherein the doped structure includes a first portion and a second portion spaced apart from and laterally surrounding the first portion;

forming a well region of the same conductivity type as the semiconductor substrate over the doped structure; and

fabricating a transistor upon and within the well region, wherein the first portion of the doped structure underlies the transistor.

15. The method as recited in claim 14, further comprising forming a doped annular region laterally surrounding and having opposite conductivity type to the well region, wherein the doped annular region overlies and contacts the second portion of the doped structure, and wherein the doped annular region laterally surrounds the transistor.

16. The method as recited in claim 15, further comprising forming metallization adapted to connect the doped annular region and the well region to opposite polarities of a supply voltage.

17. An integrated circuit, comprising:

a transistor formed in a well region of a semiconductor substrate, wherein the well region is of the same conductivity type as the substrate;

a buried layer formed within the substrate below the well region, wherein the buried layer is of opposite conductivity type than the well region;

a doped annular region extending through the well region to contact the buried layer, wherein the doped annular region is of the same conductivity type as the buried layer; and

metallization adapted to connect the well region to one polarity of a supply voltage for the integrated circuit, while precluding connection of the doped annular region to the other polarity of the supply voltage.

18. The integrated circuit as recited in claim 17, wherein the metallization is adapted to preclude connection of the doped annular region to any supply voltage of the integrated circuit.

19. The integrated circuit as recited in claim 17, wherein the metallization is adapted to connect the well region and doped annular region to the same polarity of the supply voltage.

20. The integrated circuit as recited in claim 17, wherein the transistor is an output transistor of the integrated circuit.

21. The integrated circuit as recited in claim 17, further comprising one or more analog circuit portions.

22. A method for forming an integrated circuit, said method comprising:

forming an well region over a doped structure within a semiconductor substrate, wherein the doped structure has opposite conductivity type than the substrate and the well region is of the same conductivity type as the substrate;

forming a doped annular region laterally surrounding the well region to contact the doped structure, wherein the doped annular region is of the same conductivity type as the doped structure;

fabricating a transistor upon and within the well region, wherein the transistor is laterally surrounded by the doped annular region; and

forming metallization adapted to connect the well region to one polarity of a supply voltage for the integrated circuit, while precluding connection of the doped annular region to the other polarity of the supply voltage.

23. The integrated circuit as recited in claim 10, further comprising a depletion region bridging the separation between the first and second portions of the buried layer, during times in which the well region and the doped annular region are connected to said opposite polarities of the supply voltage.

24. The integrated circuit as recited in claim 23, wherein the depletion region bridges the separation at a lower end of the buried layer.

25. The integrated circuit as recited in claim 23, wherein the depletion region increases noise isolation between the well region and the substrate.

26. The integrated circuit as recited in claim 14, wherein said forming a doped structure comprises performing a high-energy ion implantation.

27. The integrated circuit as recited in claim 26, wherein said performing a high-energy ion implantation comprises using an implant energy greater than or equal to approximately 1 MeV.

28. The integrated circuit as recited in claim 14, wherein said forming a well region comprises growing an epitaxial layer over the doped structure.